UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/996,446	11/28/2001	Daniel F. Downey	VRO-004.01	2412

7590 07/13/2004

GARY L. LOSER
VARIAN SEMICONDUCTOR EQUIPMENT ASSOCIATES, INC.
35 DORY ROAD
GLOUCESTER, MA 01930

EXAMINER	
HOLLINGTON, JERMELE M	
ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 07/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/996,446	DOWNEY ET AL.	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *9-17 and 19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,18 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 November 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. This application contains claims 9-17 and 19 drawn to an invention nonelected with traverse in the reply filed on July 1, 2003. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a) because they fail to show a resonant cavity [page 8, line 15], magnetron source [page 8, line 18], magnetic flux with a spiral copper antenna [page 9, line 3], power supply [page 9, line 3], and a ceramic chuck [page 9, line 6] as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 5-8, 18 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Maekawa (6066547).

Regarding claim 1, Maekawa discloses [see Figs. 9-11] a method for annealing a semiconductor structure (semiconductor compound 30 which includes transition metal film 24 and amorphous film 14) [see col. 6, lines 30-35], the method comprising, subjecting the semiconductor structure (30) to an oscillating electromagnetic field [see col. 6, lines 49-67] and, applying a low temperature rapid thermal annealing (LTRTA) process to the semiconductor structure (30) [see col. 6, line 57-col. 7, line 18].

Regarding claim 2, Maekawa discloses wherein subjecting includes subjecting the semiconductor to a time-varying electromagnetic field [see col. 6, lines 8-67].

Regarding claim 5, Maekawa discloses wherein applying a LTRTA includes exposing the semiconductor (30) to a temperature less than approximately 800 degrees Celsius [prior art discloses between 650-800 as shown in col. 7, lines 7-12].

Regarding claim 6, Maekawa discloses wherein applying a LTRTA includes exposing the semiconductor to a furnace having a temperature greater than approximately 500 degrees Celsius, and less than approximately 800 degrees Celsius [prior art discloses between 650-800 as shown in col. 7, lines 7-12].

Regarding claim 7, Maekawa discloses wherein applying a LTRTA can precede subjecting the semiconductor to an electromagnetic field [see col. 6, lines 8-67].

Regarding claim 8, Maekawa discloses wherein applying a LTRTA includes using a furnace to perform the LTRTA [see col. 9, lines 17-19].

Regarding claim 18, Maekawa discloses [see Figs. 9-11] a method for processing a semiconductor structure (semiconductor compound 30) comprising a subjecting the semiconductor structure (30) to a thermal heating [prior art discloses heating between 250-470

degrees Celsius as shown in col. 6, lines 57-63], and applying a low temperature rapid thermal annealing (LTRTA) process to the semiconductor structure (30) [see col. 7, lines 1-18].

Regarding claim 20, Maekawa discloses the step of subjecting the semiconductor structure (30) to an oscillating magnetic field to anneal the semiconductor structure (30) [see col. 6, lines 30-67].

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maekawa (6066547).

Regarding claims 3-4, Maekawa discloses [see Figs. 9-11] a method for annealing a semiconductor structure (semiconductor compound 30) [see col. 6, lines 30-35]. However, he does not disclose providing a frequency in a microwave frequency band or the radio frequency

(RF) band. It is well known to provide any frequency range in a frequency band where needed (see MPEP 2144.04 *In re Seid*, 161 F.2d 229, 73 USPQ 431 (CCPA 1947). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to subject the semiconductor structure to any frequency range since the frequency range, which involves matters relating to ornamentation only which have no mechanical function, would provide support in a selective manner to each individual user for annealing a semiconductor structure.

Conclusion

8. Applicant's arguments filed March 29, 2004 have been fully considered but they are not persuasive.

The applicants' argue: *"...Maekawa does not suggest or imply a method for curing structural defects, activating the dopant material, repairing the lattice structure and minimizing differences between the as implanted junction depth and the post annealing junction depth as recited by the method in claims 1 and 18 or the present application."*

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., curing structural defects, activating the dopant material, repairing the lattice structure and minimizing differences between the as implanted junction depth and the post annealing junction depth) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Base on the above argument by the examiner, the following is being given.

9. **THIS ACTION IS MADE FINAL.** Applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (517) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jermele M. Hollington
Examiner
Art Unit 2829

JMH
July 7, 2004

David A. Zarneke
Primary Exam
7/8/04